This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Canceled)

Claim 2 (Currently amended): An apparatus ~~as recited in claim 1~~ comprising:

a substrate having first and second opposite edges;

a plurality of memory devices disposed on the substrate;

a plurality of channels extending between the opposite edges, wherein each memory device of the plurality of memory devices is coupled to one channel of the plurality of channels; and

electrical contacts at the opposite edges of the substrate configured to allow communications through the channels via the electrical contacts, wherein the substrate has a first side and a second side, the plurality of memory devices being disposed on both sides of the substrate.

Claim 3 (Currently amended): An apparatus ~~as recited in claim 1~~ comprising:

a substrate having first and second opposite edges;

a plurality of memory devices disposed on the substrate;

a plurality of channels extending between the opposite edges, wherein each of the plurality of memory devices is coupled to one of the plurality of channels; and

electrical contacts at the opposite edges of the substrate configured to allow communications through the channels via the electrical contacts, wherein the substrate has a first side and a second side, the plurality of channels extending across both sides of the substrate.

Claim 4 (Currently amended): An apparatus as recited in claim [[1]]2 wherein each channel includes a plurality of conductors, the plurality of conductors following a substantially linear path across the substrate.

Claim 5 (Currently amended): An apparatus as recited in claim [[1]]2 wherein each channel includes a plurality of conductors, the plurality of conductors having lengths that are approximately equal.

Claim 6 (Currently amended): An apparatus as recited in claim [[1]]3 wherein both sides of the substrate [[has]]ve ~~one or more surfaces and the~~ memory devices [[are ]]mounted on themsuch ~~one or more surfaces of the substrate~~.

Claim 7 (Canceled)

Claim 8 (Currently amended): An apparatus as recited in claim [[7]]15 wherein the coupling of the first channel portion to the second channel portion through the connector forms a channel.

Claims 9-10 (Canceled)

Claim 11 (Currently amended): An apparatus as recited in claim [[7]]15 wherein the first channel portion includes a plurality of conductors following a substantially linear path across the first substrate.

Claim 12 (Currently amended): An apparatus as recited in claim [[7]]15 wherein the second channel portion includes a plurality of conductors following a substantially linear path across the second substrate.

Claim 13 (Currently amended): An apparatus as recited in claim [[7]]15 wherein the first channel portion includes a plurality of conductors having lengths that are approximately equal.

Claim 14 (Currently amended): An apparatus as recited in claim [[7]]15 wherein the second channel portion includes a plurality of conductors having lengths that are approximately equal.

Claim 15 (Currently amended): An apparatus as ~~recited in claim 7~~ comprising:

a first substrate having a plurality of memory devices disposed thereon and a first channel portion extending across the first substrate, the first substrate having opposite ends and contacts at the opposite ends to allow communications through the first channel portion via the contacts at the opposite ends of the first substrate;

a second substrate having a plurality of memory devices disposed thereon and a second channel portion extending across the second substrate, the second

substrate having opposite ends and contacts at the opposite ends to allow communications through the second channel portion via the contacts at the opposite ends of the second substrate;

a first connector configured to communicatively couple the first channel portion to the second channel portion through at least some of the contacts of the first and second substrates, wherein the first connector engages contacts at a first of the ends of the first substrate and engages contacts at a first of the ends of the second substrate, and

~~further including~~ a third substrate coupled to the first connector.

Claim 16 (Original): An apparatus as recited in claim 15 wherein the third substrate includes a third channel portion extending across the third substrate.

Claim 17 (Original): An apparatus as recited in claim 15 wherein the third substrate includes a third channel portion extending across the third substrate, the third channel portion including a plurality of conductors following a substantially linear path across the third substrate.

Claim 18 (Original): An apparatus as recited in claim 15 wherein the third substrate includes a third channel portion extending across the third substrate, the third channel portion including a plurality of conductors having lengths that are approximately equal.

Claim 19 (Currently amended): An apparatus as recited in claim [[7]]15 further including a second connector that engages contacts at a second of the ends

of the first substrate and engages contacts at a second of the ends of the second substrate.

Claim 20 (Original): An apparatus as recited in claim 19 wherein the second connector is coupled to a motherboard.

Claims 21-24 (Canceled)

Claim 25 (Currently amended): A method as recited in claim [[24]]30 further including propagating signals through the channel.

Claim 26 (Currently amended): A method as recited in claim [[24]]30 further including arranging a plurality of memory devices on the substrate such that each memory device is coupled to a channel portion.

Claim 27 (Original): A method as recited in claim 26 further including propagating signals through the channel portions to perform memory operations.

Claim 28 (Currently amended): A method as recited in claim [[24]]30 wherein each channel portion includes a plurality of conductors, each of the conductors having approximately equal lengths along the entire length of the channel portion.

Claim 29 (Currently amended): A method as recited in claim [[24]]30 wherein each channel portion includes a plurality of conductors following a substantially linear path across the substrate.

Claim 30 (Currently amended): A method ~~as recited in claim 24~~ comprising:

arranging channel portions on a substrate such that the channel portions extend between opposite edges of the substrate;

arranging contacts at the opposite edges of the substrate to allow communication between the contacts at the opposite edges through the channel portions;

arranging channel portion conductors such that the length of the channel portion conductors between opposite edges of the substrate is approximately equal; and

coupling together a pair of such substrates using a connector, a channel extending across the pair of substrates and the connector, wherein channel portions are arranged on both sides of the substrate.

Claims 31-34 (Canceled)

Claim 35 (Currently amended): A memory module ~~as recited in claim 34,~~ comprising:

a substrate having opposite ends and at least one surface;

contacts at the opposite ends of the substrate;

one or more memory devices mounted to the surface of the substrate; and

one or more communication channel portions extending across the module between the contacts, the one or more communication channel portions being configured to allow communications through the contacts with the one or more memory devices, wherein the substrate has opposing surfaces, and the one or more memory devices comprise at least one memory device mounted on each of the opposing surfaces of the substrate.

Claim 36 (Currently amended): A memory module ~~as recited in claim 34,~~ comprising:

a substrate having opposite ends and at least one surface;

contacts at the opposite ends of the substrate;

one or more memory devices mounted to the surface of the substrate; and

one or more communication channel portions extending across the module between the contacts, the one or more communication channel portions being configured to allow communications through the contacts with the one or more memory devices, wherein the substrate has opposing surfaces, and the one or more communication channel portions comprise at least one communication channel portion extending across each of the opposing surfaces of the substrate.

Claim 37 (Currently amended): A memory module as recited in claim [[34]]36, wherein each communication channel portion comprises a plurality of conductors that follow a substantially linear path across the substrate.

Claim 38 (Currently amended): A memory module as recited in claim [[34]]36, wherein each communication channel portion comprises a plurality of conductors having lengths that are approximately equal.